In the Specification:

Please amend the fifth paragraph on page 5 of the specification as follows:

When the disk-controller receives a Read-Command from the host system, the disk-controller studies the above parameters and determines if the first data-block in the host-data-request is the same [[a]] as the starting data-block in the cache memory (i.e, TFA = SA).

Please amend the first partial paragraph on page 6 of the specification as follows:

then determines if all of the host-data-request (i.e. TL) is in the cache memory. If it is, the disk-controller initiates auto-transfer. If it is not, then concurrent auto-transfer and microprocessor-controlled storage device transfer occur.

Please amend the first full paragraph on page 9 of the specification as follows:

Auto-transfer mechanism 113 then initiates the auto-transfer of host-requested-data from cache memory 120 to host system 150, using these three new values, i.e. using a_new value CTR' for the Buffer-Counter, using a new value SA; for the Start-Address, and using a new value [[PTR]] PTR' for the Buffer-Pointer.

Please amend the third paragraph on page 9 of the specification as follows:

When first-circuit 111 detects that the entirety of the host-requested-data is not in cache memory 120 (see 514 of FIGURE 4), controller 110 invokes microprocessor 130 (see microprocessor interface 211 of [[GIGS.]] FIGS. 2 and 3) to transfer the missing data

from storage device 140 to cache memory 120 and then to host system 150, concurrently with the other host-requested-data being auto-transferred to host system 150 from cache memory 120 by operation of auto-transfer mechanism 113.

Please amend the first full paragraph on page 11 of the specification as follows:

Host interface 210 also retrieves the ~~contact~~ content of Buffer-Counter 310 (i.e. CTR = 5), Start-Address 311 (i.e. SA = 2), and Buffer-Pointer 312 (i.e. PTR= block-2) from registers 212.

Please amend the first paragraph on page 13 of the specification as follows:

In the example illustrated in FIGURE 3, cache memory 120 contains four blocks of data, i.e. block-2 through block-5. The host-requested-data, however, starts at block-3 and includes a total of six [[block]] blocks of data, i.e. the host-requested-data comprises block-3-through-block-8. Thus, cache memory 120 contains only the portion block-3-through-block-5 of the host-requested-data.

Please amend the third paragraph on page 13 of the specification as follows:

Host interface 210 also generates the new values CTR', SA', and PTR', as above ~~describe~~ described, to replace the original values of CTR – 4, SA = 2, and PTR = 2.

Please amend the fifth paragraph on page 14 of the specification as follows:

Comparator-circuit 402 generates a second-output 505 only when the value of [[CRT]] CTR 310 is greater than the quantity TFA – SA. The presence of second-output 505 is

defined by the on-state of second-output 505, whereas the absence of second-output 505 is defined as the off-state of second- output 505. As will be apparent, the

Please amend the second full paragraph on page 15 of the specification as follows:

A second subtraction-circuit 404 is operationally coupled to switching circuit 403 to receive third-output 510 as a first input. Subtraction-circuit 404 also receives the output 503 of the Buffer-Counter [[210]] 310, i.e. the initial value of CTR, as a second input. Subtraction-circuit 404 operates to generate a fourth-output 511 equal to the initial value of CTR minus the value of third-output 510.

Please amend the second paragraph on page 16 of the specification as follows:

When second-output 505 is absent (i.e. the off-state), third-output 510 is equal to zero, and fifth-output 512 equals the quantity SA [[301]] 311, i.e. the initial value of SA is not reset.

Please amend the second paragraph on page 18 of the specification as follows:

In FIGURE 8, all of the host-requested-data 603 is again within cache memory 120 when Read-Command 300 is received by controller 110. However, in this example, the first data-block within host-requested-data 603 comprises data=6, and data-6 is not the first data block [[withi]] within cache memory 120. In this case, the values of CTR, SA, and PTR are recalculated as above described. Following this recalculation, and using the parameters TFA = 6, TL = 5, CTR' = 15, SA' = 6 and PTR' = 6, the auto-transfer of data-

6 through data 10 occurs as above described, again ~~witout~~ without invoking the assistance or microprocessor 130.

Please amend the third paragraph on page 18 of the specification as follows:

Figure 9 provides an example wherein a first-portion of host-requested-data 604 resides within cache memory 120, but a second-portion of host-requested-data 604 does not reside in cache memory 120. In this example, the first data-block within host-requested-data 604 comprises data-18. Again, data-18 is not the first data-block within cache memory 120. In this case, the values of CTR, SA, and PTR are recalculated as above described. Following this recalculation, and using the parameters TFA = 18, TL = 5, CTR' = 3, SA' = 18, the auto-transfer of data-18 through data 20 occurs as above described. However, in this example, controller 110 operates to concurrently ~~invoking~~ invoke the assistance of microprocessor 130 to fetch data-21 and data-22 from storage device 140. This operation by controller 110 is transparent to host system 150, since host system 150 receives the requested data-18 through data-22 by virtue of the concurrent auto-transfer-operation and microprocessor-fetch-operation.